AMENDMENTS TO THE CLAIMS

1. (Previously Amended) A method of forming a bipolar transistor on a wafer, the wafer having a buried layer and an epitaxial layer of a first conductivity type formed over the buried layer, the epitaxial layer having a top surface and a smaller dopant concentration than the buried layer, the method comprising the steps of:

forming a trench in the epitaxial layer;

forming a layer of base material on the epitaxial layer and the trench;

forming a layer of base protection material on the layer of base material; and

chemically-mechanically polishing the layer of base material and the layer of base protection material until the top surface of the epitaxial layer and a top surface of the layer of base protection material are substantially coplanar.

2. (Previously Amended) The method of claim 19 wherein the portion of the layer of base protection material is removed with a wet etch.

3. (Original) The method of claim 2 wherein an area and location of a base-to-collector junction is defined by the trench.

4. (Previously Amended) The method of claim 20 wherein the step of forming an isolation region includes the steps of:

forming a layer of isolation material on the epitaxial layer, the layer of base material, and the layer of base protection material; and

etching a portion of the layer of isolation material to expose a portion of the layer of base protection material.

5. (Original) The method of claim 1 wherein the layer of base material includes silicon and germanium.

6. (Original) The method of claim 1 wherein the layer of base material includes silicon, germanium, and carbon.

7. (Previously Amended) The method of claim 20 and further comprising the steps of:

forming a layer of conductive material on the portion of the layer of base material and the isolation region; and

etching the layer of conductive material to form an extrinsic emitter and an exposed base region, the extrinsic emitter contacting the layer of base material and the top surface of the isolation region.

8. (Original) The method of claim 7 and further comprising the step of planarizing the layer of conductive material prior to the step of etching the layer of conductive material.

9. (Original) The method of claim 7 wherein the step of etching the layer of conductive material is a timed etch.

10. (Previously Amended) The method of claim 7 wherein the extrinsic emitter has an end that contacts the layer of base material, the end having a substantially vertical end wall.

11. (Previously Amended) The method of claim 7 and further comprising the steps of:

etching the isolation region such that a side wall of the extrinsic emitter and a side wall of the isolation region are substantially aligned; and

forming a first layer of insulation material on the exposed base region and the extrinsic emitter.

12. (Original) The method of claim 11 wherein a width of the extrinsic emitter is less than a width of the isolation region, the width of the extrinsic emitter and the width of the isolation region being measured along a line substantially perpendicular to a plane that includes substantially all of a side wall of the extrinsic emitter.

13. (Original) The method of claim 7 wherein the layer of conductive material is polysilicon.

14. (Previously Amended) The method of claim 13 wherein the layer of conductive material is doped to have the first conductivity type.

15. (Previously Amended) The method of claim 21 wherein the step of forming an intrinsic emitter region includes the step of annealing the wafer to cause dopants to outdiffuse from the extrinsic emitter into the base material.

Claims 16-18 (Cancelled)

19. (Currently Amended) ~~The method of claim 1 and further comprising the step of~~ A method of forming a bipolar transistor on a wafer, the wafer having a buried layer and an epitaxial layer of a first conductivity type formed over the buried layer, the epitaxial layer having a top surface and a smaller dopant concentration than the buried layer, the method comprising the steps of:

forming a trench in the epitaxial layer;

forming a layer of base material on the epitaxial layer and the trench;

forming a layer of base protection material on the layer of base material; and

chemically-mechanically polishing the layer of base material and the layer of base protection material until the top surface of the epitaxial layer and a top surface of the layer of base protection material are substantially coplanar;

removing a portion of the layer of base protection material to expose a portion of the layer of base material, the base material being conductive, the base protection material being non-conductive.

20. (Previously Added) The method of claim 19 and further comprising the step of forming an isolation region on the layer of base material and the layer of base protection material.

21. (Cancelled).

22. (New) The method of claim 11 and further comprising the steps of:

forming a second layer of insulation material on the first layer of insulation material;

etching the second layer of insulation material to form an exposed region of the first layer of insulation material and a side wall spacer that adjoins the extrinsic emitter;

etching the exposed region of the first layer of insulation material to remove the first layer of insulation material from the base material;

forming an extrinsic base region in the layer of base material after the first layer of insulation material has been etched; and

forming an intrinsic emitter region in the layer of base material after the extrinsic base region has been formed.

23. (New) A method of forming a bipolar transistor on a wafer, the wafer having a semiconductor material of a first conductivity type, the semiconductor material having a top surface, the method comprising the steps of:

forming a trench in the semiconductor material;

forming a layer of base material on the semiconductor material and the trench;

forming a layer of base protection material on the layer of base material; and

chemically-mechanically polishing the layer of base material and the layer of base protection material until the top surface of the semiconductor material and a top surface of the layer of base protection material are substantially coplanar.

24. (New) The method of claim 23 and further comprising the step of forming an isolation region on the layer of base material and the layer of base protection material.

25. (New) The method of claim 1 and further comprising the step of removing a portion of the layer of base protection material to expose a portion of the layer of base material, the base material being conductive, the base protection material being non-conductive.

26. (New) The method of claim 25 and further comprising the steps of:

forming a layer of conductive material on the portion of the layer of base material and the isolation region; and

etching the layer of conductive material to form an extrinsic emitter and an exposed base region, the extrinsic emitter contacting the layer of base material and the top surface of the isolation region.

27. (New) The method of claim 26 and further comprising the steps of:

etching the isolation region such that a side wall of the extrinsic emitter and a side wall of the isolation region are substantially aligned; and

forming a sidewall spacer adjacent to the sidewalls of the extrinsic emitter over the exposed base region.

REMARKS

Reconsideration of the application in view of the above amendments and the following remarks is requested. Claims 1-15, 19-20, and 22-27 are in this application. Claim 19 has been amended. Claims 16-18 and 21 have been cancelled. Claims 22-27 have been added. Claim 22 has been added to remove any confusion associated with original claim 21. Claims 23-27 have been added to alternately and additionally claim the present invention.

Applicant requests the Examiner to provide an initialed copy of the PTO-1449 Form that was filed with the IDS on June 11, 2003, and received by the PTO on June 13, 2003. Applicant also requests the Examiner to indicate if the substitute formal drawings filed on April 29, 2003, and received by the PTO on May 5, 2003, have been accepted.

The Examiner objected to the drawings under 37 CFR §1.84(p)(4) because reference numerals 869 and 870 have both been used to designate sidewall spacers. Applicant notes that reference numeral 869 designates a portion of a second layer of isolation material, while reference numeral 870 designates the sidewall spacer that results when the second layer of isolation material is anisotropically etched. (See applicant's specification, page 17, lines 12-16.) As a result, only one of the two reference numerals, numeral 870, represents the sidewall spacer. Thus, it is believed that the drawings satisfy the requirements of 37 CFR §1.84(p)(4).

The Examiner rejected claims 1-5 under 35 U.S.C. §103(a) as being unpatentable over Kato (U.S. Patent No. 5,648,280) in view of Kameyama et al. (U.S. Patent No. 5,077,227), Fitzgerald (U.S. Patent No. 6,171,936 B1), and Boyd et al. (U.S. Patent No. 5,362,669). For the reasons set forth below, applicant respectfully traverses this rejection.

Claim 1 recites, in part,

> "forming a trench in the epitaxial layer;
> "forming a layer of base material on the epitaxial layer and the trench;
> "forming a layer of base protection material on the layer of base material; and
> "chemically-mechanically polishing the layer of base material and the layer of base protection material until the top surface of the epitaxial layer and a top surface of the layer of base protection material are substantially coplanar."

In rejecting the claims, the Examiner appears to point to the step of forming a trench 5 in substrate 1 as shown in FIG. 4E of Kato as constituting the step of forming a trench required by claim 1, except that Kato does not teach that the trench is formed in an epitaxial layer. The Examiner also appears to point to the step of forming base layer 7 in trench 5 as shown in FIG. 4F of Kato as constituting the step of forming a layer of base material as required by claim 1.

With respect to the "chemically-mechanically polishing" step, the Examiner noted that the combination of Kato and Kameyama does not disclose this step, but argued that the Fitzgerald reference teaches this limitation. As shown in FIGs. 1B and 1C, Fitzgerald teaches that silicon dioxide layer 104 and uniform SiGe layer 108 are chemically-mechanically polished until the top surface of uniform SiGe layer 108 is coplanar with the top surface of wafer 100.

The Examiner argued that it would be obvious to combine Fitzgerald with Kato and Kameyama because it would enable portions of base layer 7 of Kato to be removed. Applicant, however, has been unable to find any discussion in Kato that teaches that any portion of base layer 7 is removed, or suggests that it would be desirable to remove any portion of base layer 7. As taught by Kato in column 7, lines 18-31, base layer 7 is formed within recessed portion (trench) 5 to have a thickness that "just corresponds" to the depth of recessed portion 5.

With respect to the "forming a layer of base protection material" step, the Examiner noted that the combination of Kato, Kameyama, and Fitzgerald does not disclose this step, but argued that the Boyd reference teaches this limitation. The Examiner indicated, in part, that base material layer 160 and base protection material layer 148 (which are shown in FIG. 5 of Boyd) are chemically-mechanically polished so that a top surface of base protection material layer 148 is coplanar with a top surface of substrate 132.

Applicant notes, however, that FIG. 6 of Boyd shows that the chemical-mechanical polishing step stops when the top surface of base protection material layer 148 at the bottom of the trench, which forms a first polish stop 150 (see FIG. 5 of Boyd), is coplanar with a top surface 134 of a chemical-mechanical polish (CMP) resistant layer, which forms a second polish stop 152 (see FIG. 5 of Boyd). The top surface of base protection material layer 148 at the bottom of the trench, however, is not coplanar with the top surface of substrate 1.

In addition, the Examiner argued that one skilled in the art would be motivated to combine the teachings of Boyd with the teachings of Kato as modified by Kameyama and Fitzgerald to reduce and control the dishing associated with chemical-mechanical polishing processes. It is unclear to applicant, however, how the teachings of Boyd would be applied to Kato as modified by Kameyama and Fitzgerald to satisfy the requirements of claim 1.

Applicant notes that Kato and Boyd both have first layers of CMP resistant material in silicon nitride films 3a and 134 that are formed on substrates 1 and 132, respectively. Assume that the teachings of Boyd are applied to Kato as modified by Kameyama and Fitzgerald such that a second layer of CMP resistant material, such as layer 148 of Boyd, is deposited on layers 6 and 7 (which are shown in FIG. 4F of Kato).

In this case, it is unclear to applicant how the second layer of CMP resistant material (read to be the base protection material layer of claim 1) and base layer 7

(read to be the base material layer of claim 1) of Kato could be chemically-mechanically polished until the top surface of the second layer of CMP resistant material and the top surface of substrate 1 of Kato are substantially coplanar because the top surface of the second layer of CMP resistant material lies above the top surface of substrate 1.

Thus, since the combined teachings of Kato, Kameyama, and Fitzgerald do not teach the "forming a layer of base protection material" step of claim 1, and the further combination of Boyd does not teach the required limitations, claim 1 is patentable over Kato in view of Kameyama, Fitzgerald, and Boyd. In addition, since claim 5 depends from claim 1, claim 5 is patentable over Kato in view of Kameyama, Fitzgerald, and Boyd for the same reasons as claim 1.

The Examiner also rejected claim 6 under 35 U.S.C. §103(a) as being unpatentable over Kato in view of Kameyama et al., Fitzgerald, and Boyd et al. as applied to claims 1 and 5 above, and further in view of Chu et al. (U.S. Patent No. 6,426,265 B1). Since claim 6 depends from claim 1, and claim 1 is patentable over Kato in view of Kameyama et al., Fitzgerald, and Boyd et al. as applied above, claim 6 is patentable over Kato in view of Kameyama et al., Fitzgerald, and Boyd et al. as applied to claims 1 and 5 above, and further in view of the Chu et al. reference.

The Examiner objected to claims 19 and the claims dependent thereon, but indicated that these claims would be allowable if rewritten in independent form to include the limitations of the base claim and any intervening claims. Claim 19 has been amended to be in independent format, and is believed to include all of the limitations of base claim 1. The claims dependent thereon have not been amended to be in independent form as these claims depend from claim 19.

New claim 23 recites, in part,

> "forming a trench in the semiconductor material;
> "forming a layer of base material on the semiconductor material and the tre"nch;
> "forming a layer of base protection material on the layer of base material; and
> "chemically-mechanically polishing the layer of base material and the layer of base protection material until the top surface of the semiconductor material and a top surface of the layer of base protection material are substantially coplanar."

With respect to claim 23, it is unclear to applicant how a second layer of CMP resistant material from Boyd (read to be the base protection material layer of claim 23), which is formed on base layer 7 of Kato (read to be the base material layer of claim 23) could be chemically-mechanically polished until the top surface of the second layer of CMP resistant material and the top surface of substrate 1 of Kato (read to be the semiconductor material of claim 23) are substantially coplanar because the top surface of the second layer of CMP resistant material lies above the top surface of substrate 1.

Since the combined teachings of Kato, Kameyama, and Fitzgerald do not teach the "forming a layer of base protection material" step, and the further combination of Boyd does not does not teach the required limitations as discussed above, claim 23 is patentable over Kato in view of Kameyama, Fitzgerald, and Boyd. In addition, since claims 24-27 depend either directly or indirectly from claim 23, claims 24-27 are patentable over Kato in view of Kameyama, Fitzgerald, and Boyd for the same reasons as claim 23.

Thus, for the foregoing reasons, it is submitted that all of the claims are in a condition for allowance. As a result, the Examiner's early re-examination and reconsideration are respectfully requested.

Respectfully submitted,

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